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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/432,927	11/03/1999	JUNJI NISHIGAKI	15162/01250	1794

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EXAMINER	
GRANT II, JEROME	
ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/432,927	NISHIGAKI, JUNJI	
	Examiner	Art Unit	
	Jerome Grant II	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-12* is/are rejected.

7)☒ Claim(s) *3,6 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

JEROME GRANT II
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1.
A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 4, 5 and 7-12 rejected under 35 U.S.C. 102(a) as being anticipated by Takebe.

With respect to claim 1, Takebe teaches an image processing system (shown by figure 1), comprising: synchronous type processing means (105 or 102) for carrying out a first image process on image data (sub-image VD or main -image Vdm)) that is subject to processing;

asynchronous type processing means (asynchronous reading and writing via memories 107a, 107b) for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing and synthesize means 110 for synthesizing an output of said synchronous type processing means and an output. of said synchronous type processing means to form one image data, see col. 15, lines 47-55.

With respect to claim 2, Takebe teaches image processing system according to claim 1, wherein said synthesize means comprises: a memory 107a and 109b in which an output of said Synchronous type processing means is stored, and replacement means FIFO 108 for replacing a portion (sub-image) of an output of said synchronous type processing means (102, 105) stored in

said memory (107a, 107b) with an output of said synchronous type processing means.

With respect to claim 4, Takebe teaches an image processing system(see figure 1) comprising: a first image processor (102) formed of a hardware circuit, and carrying out a first image process on input image data; a second image processor 105 carrying out a second image process on a fragment of said input image data according to a program of predetermined software; and a memory 107a, b and 108 in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored.

With respect to claim 5, Takebe teaches the image processing system wherein data of said memory in which image data subjected to the first image process is stored is overwritten by (overwritten by other sub-or image data via 107a,b) subjected to the second image process. See also the FIFO data which is constantly overwritten since it is a read/write type of memory according to col. 16, lines 17-22.

With respect to claim 7, Takebe teaches the software is rewritable. According to Col. 16, lines 35-40, Software is rewritable in that addresses are calculated based upon scale data which is variably determined by an operator or other communication device.

With respect to claim 8, Takebe teaches, second image processor detects a region on which the second image process is to be carried out by scanning input image data. Note, second image processor 105 which scans sub-image data in an interlace fashion, i.e., odd fields then even.

With respect to claim 9, Takebe teaches an image processing method comprising the steps of carrying out a first image process (via 1021 on input image data through hardware circuit; carrying out a second image process (via circuit 105) on a fragment of the input image data through the software (i.e., sub-image data). Takebe teaches synthesizing image data (via 110) subjected to the first image process with image data subjected to the second image process,

wherein sequence of said first and second image process is arbitrary. The process are arbitrary in that the data is input independently from the other Le., asynchronously.

With respect to claim 10, Takebe teaches an image processing method according to claim 9, wherein said step of carrying out the second image process (sub-image synthesis includes the step of detecting a region on which the second image process is to be carried out (line region) by scanning input image data, and carrying out: the second image process on the detected region (second process is interlaced scanning on the sub-image).

With respect to claim 11, Takebe teaches an image processing system comprising: a

Synchronous-type data processing device (102, 105) for carrying out a first image process on image data that is the subject of processing; an asynchronous -type data processor (107a, 107b) for carrying out a second image process ort image data of a predetermined region of said image data that is the subject of processing, see col. 15, line 65 - col. 16, line 2. Takebe teaches a data synthesizing device (110) for synthesizing ,an output of said synchronous-type processing device and an output(selector 104) of said asynchronous-type processor to thereby form on image data (displayed on display 109).

With respect to claim 12, Takebe teaches an image processing system according to claim 11, where the synthesizing device includes: a memory (108) for storing an output of said

Synchronous-type processing device, and wherein said synthesizing device 110 replaces a portion of an output of said synchronous-type processing device stored in said memory with an output of said asynchronous-type processor (via FIFO 108).

2.

Claims Objected

Claims 3, 6 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's Response

Applicant argues that Takebe does not disclose any processing. Yet the examiner referred to an image processing system according to figure 1. Applicant has not provided a rationale that would explain why figure 1 is not an image processing system. Hence, applicant has not met the burden of disproving Takebe as having an image processing system.

Applicant argues that elements 102 and 105 do not process image data. Perhaps elements 102 and 105 do not process data in the specific manner as explained in the written specification. None-the-less, 102 and 105 together broadly functions as a means for processing for the reasons provided in the claim. Because 102 and 105 do process data, it is broad enough to read on the claimed structure.

With respect to the comment that memories 107a/b are not asynchronous circuitry, the examiner contends that the writing of the memories and not the memories themselves constitute an asynchronous function.

Applicant argues that Takebe fails to teach a synchronous or asynchronous processing means. The examiner had explained that the synchronous operation, was executed by means of elements 105 and 102 ad the asynchronous operation was executed by means of the reading and writing from memories 107a and 107b. Applicant has provided no rationale as to why the proposed elements advanced by the examiner do not meet the specifics of the claims, namely asynchronous and synchronous modes of operation.

With respect to claim 2, applicant makes the same argument with regard to the synchronous and asynchronous operation. The same response to this argument as provided in the proceeding argument applies here.
Applicant further argues that Takebe fails to provide a single path from the alleged synchronous processing means to the alleged memory. But upon closer view, there is no language in the claim that insinuates or makes specific reference to a signal path from the synchronous processor to the alleged memory.

Applicant argues that Takebe does not provide a memory in which an output of said synchronous type processing means is stored. The examiner had provided that 107a ad 109b meet this claimed requirement. But in the argument, applicant has not provided an argument as to why elements 109 b and 107a do not function as the claim purports. Hence, applicant has not satisfactorily traversed the rejection.

With respect to claim 4, applicant argues that Takebe fails to disclose processing of image data. This is a mere allegation. No facts have been presented in support for this assertion. The examiner referred to the image processing system of figure 1 as having addressed the claimed limitation.

Applicant argues that Takebe does not teach memory in combination with a main and subimage. Claim 4 does not recite storing a main and a sub-image data. Thus, applicant is arguing limitations which are not supported in the claim. Takebe does teach synthesizing first and second data via circuit 108. Applicant has not provided a rationale as to why the abovementioned elements could not function as the elements intended in the claim.

With respect to claim 5, applicant argues that Takebe fails to teach first image processing that was stored is overwritten by image data subjected to the second image process. This is a mere allegation. No evidence has been provided in support for applicant's position. The reference teaches that the FIFO data which is constantly overwritten since it is a read/write type of memory according to col. 16, lines 17-22.

With respect to claim 7, applicant alleges that Takebe does not disclose software that is re-writable. The examiner notes that applicant has not provided evidence in support for this contention. According to col. 16, lines 35-40, software is rewritable in

that addresses are calculated based upon scale data which s variably determined by an operator or other communication device.

With respect to claim 8, applicant alleges that Takebe fails to disclose that "said second image processor detects a region on which the second image processing to be carried out by scanning input image data." Applicant has not provided a reason why the limitations relied upon by the examiner do not meet the claimed feature. The examiner submits the second image processor detects a region on which the second image process is to be carried out by scanning input image data. Note, second image processor 105 scans sub-image data in interlace fashion."

Regarding claim 9, applicant alleges that Takebe does not provide any image processing through a hardware circuit.. The hardware circuit for carrying out this function is element 1021. Applicant has not provided a reason why this element does not perform the function as claimed.

With respect to claim 10, applicant argues that Takebe does not identify an image area to be processed and detecting a region for a second image processed. Takebe teaches carrying the second image process (sub-image synthesis includes the step of detecting a region on which the second image process is to be carried out (line region) by scanning input image data, and carrying out."

With respect to claims 11 and 12, these arguments have been presented in response to the comments to claims 1 and 2 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Grant II whose telephone number is 571-272-7463. The examiner can normally be reached on Mon.-Thur. From 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A Williams, can be reached on 571-272-7471. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Grant II

JEROME GRANT II
PRIMARY EXAMINER